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PATENTS
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Applicants	:	Tony K. Ngai et al.
Application No.	:	09/124,649
Filed	:	July 29, 1998
For	:	PROGRAMMABLE LOGIC DEVICE HAVING EMBEDDED DUAL-PORT RANDOM ACCESS MEMORY CONFIGURABLE AS SINGLE-PORT MEMORY
Group Art Unit	:	2752
Examiner	:	Pierre-Michel Bataille

New York, New York 10020
October 20, 2000

Hon. Commissioner for Patents
Washington, D.C. 20231

PETITION UNDER 37 C.F.R. §1.136(a)
FOR EXTENSION OF TIME AND
REPLY TO OFFICE ACTION

Sir:

Petition Under 37 C.F.R. § 1.136(a)
For Extension of Time

Pursuant to 37 C.F.R. § 1.136(a), applicants hereby petition for a two-month extension of the shortened statutory period set for reply to the Office Action dated June 12, 2000, to make the date for reply November 12, 2000. A check in the amount of $390.00, in payment of the fee set forth in 37 C.F.R. § 1.17(a)(2), is enclosed herewith. The Director is hereby authorized to charge any additional fee that may be due, or credit any overpayment, in connection with this Petition and Reply, to Deposit Account No. 06-1075. A duplicate copy of the transmittal letter accompanying this Petition and Reply, authorizing the deposit account transaction, is enclosed herewith.

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Reply to Office Action

In reply to the Office Action dated June 12, 2000, applicants hereby amend the above-identified patent application as follows:

In the Drawings

Please approve the following amendments of FIG. 1, as indicated in red on the attached copy, so that corrected formal drawings may be filed:

Please insert the legend "OUTPUT NETWORK" where shown (5 occurrences);

Please insert the legend "I/O PIN" where shown (9 occurrences);

Please insert the legend "PROGRAMMABLE LOGIC REGION 12" where shown.

REMARKS

Summary of Office Action

Claims 1-12 are pending in the above-identified patent application.

The Examiner has rejected claims 1-12 under 35 U.S.C. § 102(e) as being anticipated by Heile U.S. Patent 6,020,759. Claims 3-6 and 9-12 have been objected to under 37 C.F.R. § 1.75(c) as being of improper dependent form. The drawings have been objected to under 37 C.F.R. § 1.83(b) as allegedly being incomplete. The declaration has been objected to as allegedly being defective.

Summary of Applicants' Reply

Applicants have proposed amending FIG. 1 of the drawings. The Examiner's objections and rejection are respectfully traversed.

Applicants' Reply to the Objection to the Declaration

The declaration filed with the above-identified patent application has been objected to as allegedly being defective for not identifying the citizenship or residence of each inventor. This objection is respectfully traversed.

The declaration filed with the above-identified patent application states, in the first paragraph:

> We, Tony K. Ngai, Rakesh H. Patel, Srinivas T. Reddy, and Richard G. Cliff, declare that we are citizens, respectively, of Canada, the United States of America, India, and the United States of America, respectively residing and having post office addresses at 2830 Gazelle Drive, Campbell, California 95008, 20087 Las Ondas Court, Cupertino, California 95104, 2289 Camellia Court, Fremont, California 94539, and 194 Smithwood Street, Milpitas, California 95035.

The above-quoted paragraph identifies the citizenship, residence and post office address of each applicant. Accordingly, applicants respectfully request that the objection to the declaration be withdrawn.

Applicants' Reply to the
Objection to the Drawings

The drawings have been objected to under 37 C.F.R. § 1.83(b) as allegedly being incomplete, because certain boxes, while identified by reference numeral, were not labelled. The Examiner's stated basis for this objection was that the drawings should be understandable without reference to the text. This objection is respectfully traversed.

Applicants are aware of no requirement in the rules that the drawings should be understandable without reference to the text. Nevertheless, in order to advance prosecution of this application, applicants have proposed amending FIG. 1 as suggested by the Examiner, to label boxes 100, 101 and 12. However, because the boxes in question are small, applicants propose labelling the boxes outside the boxes themselves, in association with the reference numerals for the boxes. Because of space

constraints, not all occurrences of the relevant reference numerals are proposed to be labelled.

Applicants respectfully request that the Examiner approve the proposed amendments of FIG. 1, indicated in red on the attached copy, so that corrected formal drawings may be filed.

Applicants' Reply to the
Objection to Claims 3-6 and 9-12

Claims 3-6 and 9-12 have been objected to under 37 C.F.R. § 1.75(c) as being of improper dependent form. This objection is respectfully traversed.

Independent claims 1 and 7 define, respectively, a programmable logic device ("PLD") and an integrated circuit ("IC"). Claims 3 and 9 define a digital processing system respectively incorporating, inter alia, the PLD of claim 1 or the IC of claim 7. Claims 4-6 and 10-12 define a printed circuit board respectively incorporating, inter alia, the PLD of claim 1 or the IC of claim 7. The basis of the Examiner's objection is not clear, but he seems to be objecting to the fact that the independent and dependent claims are drawn to different types of products. However, MPEP § 608.01(n)(III) explicitly permits such dependent claims. For example, in the context of discussing a method claim that depends from a product claim, that section states that "if claim 1 recites a specific product, a claim for the method of making the product of claim 1 in a particular manner would be a proper dependent claim."

According to MPEP § 608.01(n)(III), the only valid test for the propriety of a dependent claim is whether or not the dependent claim could conceivably be infringed by something that would not infringe the independent claim. That is not the case here; any digital processing system incorporating the device of claim 1 or 7, which therefore falls within claim 3 or 9, also would inherently infringe claim 1 or 7. Similarly, any printed circuit board having thereon the device of claim 1 or 7, which therefore falls

within one of claims 4-6 or one of claims 10-12, also would inherently infringe claim 1 or 7.

Accordingly, applicants respectfully submit that claims 3-6 and 9-12 are proper dependent claims, and respectfully request that the objection to claims 3-6 and 9-12 be withdrawn.

Applicants' Reply to the
Prior Art Rejection

Claims 1-12 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Heile U.S. Patent 6,020,759. This rejection is respectfully traversed.

Applicants' invention is an integrated circuit, such as a programmable logic device, having programmable resources for interconnecting components thereon, and including a dual-port random access memory ("RAM") that is configurable as a single-port RAM. A single-port RAM is a RAM that has one port for both reading and writing, while a dual-port RAM is a RAM that has separate read and write ports. As result, at any one time, a single-port RAM can either be read from or written to, but a dual-port RAM can be read from and written to simultaneously. Inherently, if the same addressing scheme and data word size is used for both reading and writing even in a dual-port RAM, both ports of a dual-port RAM are the same size -- i.e., have the same number of conductors.

In order to provide maximum flexibility for users, in a programmable logic device on which user-accessible RAM is provided, it would be desirable to be able to configure the RAM as either single-port RAM or dual-port RAM. One way to achieve that flexibility is to actually provide both types of RAM on the device, allowing the user to access whichever type is needed. A more efficient way, however, is to provide only one type of RAM, but to provide the resources necessary to configure it as either type of RAM. According to the present invention, dual-port RAM is provided on the device.

If dual-port RAM is to be configured as single-port RAM, then every conductor in the read port of the dual-port RAM ordinarily would have to be connected in parallel with the corresponding conductor in the write port. However, the connections of the various inputs and outputs to the two separate ports may, and usually do, pass through different programmable interconnection resources of the programmable device. In most contemporary programmable logic devices, not all interconnection resources are "fully populated" -- i.e., if an interconnection resource programmably connects two groups of conductors, not all conductors in one group of conductors can be connected to every conductor in the other group of conductors. Therefore, in accordance with the present invention, the device is constructed so that the interconnection resources needed to connect to the two ports are sufficiently populated to allow simultaneous connection to corresponding conductors in both ports.

Heile neither shows nor suggests the claimed invention. Heile shows a dual-port RAM that is configurable as a product-term ("p-term") logic module. As such, Heile is concerned with the addressing of the RAM, because in p-term mode, it may be necessary to address several rows of the RAM at once, while in normal RAM operation, rows are addressed individually. The portion of Heile to which the Examiner points as showing the inventive feature of the present claims discusses only the re-routing of the normal read address lines to the p-term inputs, while the present invention is the provision of sufficient connections to allow corresponding conductors in the two ports to be connected simultaneously to the same input/output conductor. There is no teaching or suggestion of the claimed invention in Heile, either in the portions identified by the Examiner or anywhere else.

Turning to the specific elements of applicants' claims as identified by the Examiner, the Examiner correctly equates the claimed plurality of interconnection conductors

with conductor network 23 of Heile. The Examiner then purports to identify the claimed plurality of programmable interconnection resources -- for connecting conductors of the interconnection conductors 23 to the plurality of logic resources 21, and including the claimed first and second programmable interconnection resources -- with the decoders and multiplexers 13, 18, 19, 103 and 107. However, even if those decoders and multiplexers had all of the other characteristics that the claims require of the claimed programmable interconnection resources (and they do not, as discussed below), the decoders and multiplexers do not connect to the interconnection conductors 23, but rather to conductors within RAM module 10.

Finally, the Examiner points to column 3, line 50 through column 4, line 12 of Heile as supporting the claimed limitations on the degree to which the first and second programmable interconnection resources are populated. As discussed above, this portion of Heile discusses only the re-routing of the normal read address lines to the p-term inputs, neither of which connects to either the read port or the write port as do the claimed first and second programmable interconnection resource.

An anticipation rejection under any subsection of 35 U.S.C. § 102, including Section 102(e), requires that all of the limitations of applicants' claims be found in the allegedly anticipating reference. Applicants have shown that Heile does not show all of the elements of applicants' claims. And as discussed above, Heile also does not suggest applicants' invention.

For these reasons, applicants respectfully submit that the claimed invention is patentable.

Conclusion

For the reasons set forth above, applicants respectfully submit that this application, as amended, is in

condition for allowance. Reconsideration and prompt allowance of this application are respectfully requested.

Respectfully submitted,

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on October 20, 2000

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